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X 77-Design and Construction of a 16-bit Microcomputer System using Bit-Slice Microprogrammable Microprocessor

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Introduction

The purpose of the present report is to describe a continuing research and development program, called X77, concerned with a design and construction of a general purpose mini-level digital computer system using new hardware and software technology, which has been pursued since 1975 as a part of an on-going microprocessor application research termed Project Micro for short at KAIS. Other aspects of Project Micro ranging from those dealing with specific microprocessor applications within the context of commercial products to experiences in design, implementation and use of various software support and teaching aid for microprocessor applications, such as P8076 package for cross-assembly and simulation related to 8080 microprocessors with a Nova 16—bit minicomputer facility as a host, are to be described elsewhere.

The microprocessor technology is relatively new, being no more than say five years old, but as is well known, it is already establishing itself as a major new era in the evolutionary sequence of digital design methods, namely those based on vacuum tubes, transistors, fixed-function integrated circuits and finally microprocessors — programmable general purpose LSI circuits — respectively. In view of economics as well as technical factors, such as enhanced design flexibility (inherent in programming) and increased product reliability (due to reduced component count), it has become evident that the conventional approach of "hard-wired" random logic design will largely become obsolete to be superceded by the new technique of "programming" general purpose LSI processors.

Combined with the rapid progress in the development of LSI circuits — as evidenced by memory chips consistently doubling the capacity in every year or two for last several years and continuing and by improved processors and other support circuits frequently announced industry-wide — hand-in-hand with circuit price reductions with a pace no less drastic, the new technique is affecting in a fundamental way the entire spectrum of digital design, ranging from "intelligent" devices, e.g., auto-ranging digital multimeters, programmed electronic games to various subsystems including central processing units, input/output device controllers, remote terminals, etc., of general purpose computer systems. A recent survey of microprocessor technology can be found in an article by the present author, which contains a list of references pertaining to microprocessors.

1. Intel 3000 Series Bipolar Microcomputer Set.

The research and development effort, X77, being reported on was undertaken to investigate the characteristics of a microprogrammed CPU using the new technique based on bipolar LSI bit-slice microprogrammable microprocessors. The formative idea on X77 began when the author attended one of Intel seminars in early 1975 introducing Intel Series 3000 Bipolar Microcomputer Set[2], the first one of such class having the following features:

1. Schottky bipolar with an attainable speed of 150 to 200 nsec for microinstruction cycle time at system level,
2. bit-slice architecture for cascading to a user-specified word length, and
3. microprogrammable.

These characteristics make the 3000 set suitable building blocks for implementing a general purpose CPU of a mini-level computer system with a 16-bit wide data path and (macro) instruction cycle times of a few μ secs.

2. National Semiconductor 16-bit Microprocessor PACE.

Even a mini-level computer system, of course, consists of many diverse subsystems, hardware as well as software, the CPU being merely one such hardware component. Rather than embarking on an architecture of a new design totally disjoint from any of the existing systems, it was decided to emulate one of the known 16-bit minicomputer CPU. For this purpose PACE[3], a 16-bit single-chip microprocessor from National Semiconductor Corp., was selected on the following ground:

1. PACE being comparatively newer in design has a more advanced architecture and powerful instruction set than any of the well known and widely available minicomputers of older generation,
2. The instruction set of PACE is organized in a more systematic manner than those of others based on the conventional random logic design.
3. PACE being a PMOS processor has a nominal execution speed (8.5 μ sec minimum instruction cycle time) which is significantly slower than those of prevalent NMOS processors.[4] Thus a high speed version appeared interesting.[5]

3. Design Approaches and Engineering Techniques.

As mentioned earlier the pace of progress in LSI technology is extremely fast and accelerating For this reason, from a short as well as long range point view, design approaches taken and engineering methods developed, the means for short, probably have a longer lasting value than the end to be attained. Thus throughout X77 from its inception to actual constructions a greater emphasis has been placed on the development of general purpose tools and techniques, used in design, construction and techniques used in design, construction and debugging of various subsystems. A brief description of this aspect of X77 follows.

3.1 Software Support.

The software tools require, for both their implementation and use, a general purpose computing facility. For such purpose KAIS had readily available (a batch access to) a minicomputer facility consisting of a NOVA 840 16-bit computer with 32K word of core and various pheripheral devices running under a discbased operating system, the languages supported including FORTRAN IV and (extended) ALGOL.

On the other hand, most of commercially available software packages — so far only cross-assemblers and none for simulating bit-slice microprogrammable microprocessors are known —, even if available in source form, say in FORTRAN for "portability", are intended for use on a large computing facility requiring a word size of 32 bits or more. Experiences show that adapting such a package to a 16-bit minicomputer is well nigh impossible in practice. For this reason some of the software tools mentioned below had to be designed and implemented for the KAIS NOVA facility from scratch and required a substantial effort in subsequent debugging. They include:

1. S3076 (in ALGOL) which simulated in the form of "logic blocks" various LSI circuits of the 3000 set. Based on S3076 the entire CPU design of X77 was simulated on NOVA at the level of logic blocks including microinstruction pipe-lining, all user-defined microfunctions for bus control, and ancillary circuits for macroinstruction decoding.

2. A3076 (in FORTRAN), a cross-assembler for microprogramming identical in language and similar in function to XMAS of Intel CROMIS package[6], which was used to write the microcode for X77.

Concerning a commercial package the following experience may be illuminating. Since CROMIS package is available for purchase in source form for a moderate cost, what justifies the effort in A 3076? Project Micro, in fact, subsequently

acquired CROMIS package from Intel, which came in the form of two 2400 ft tapes containing the information for installation and operation as FORTRAN comment cards together with the source programs. To extract from these tapes the documentation parts and to separate each program in a manageable form the author had to resort to an interactive text-editing using over 160 tracks of on-line disc pack of a large computing center, viz., the IBM (2) 370/168 - (1) 360/91 triplex facility of Stanford Linear Accelerator Center, Stanford University.

For example the microassembler, XMAS (Version 2.0, May, 1975), one of two major parts of CROMIS, consisted of nearly 28,000 lines of FORTRAN source, of which about 11,000 lines were coded. Compiling this source (after eliminating all comment cards) using IBM OS FORTRAN IV (H) compiler took about a minute of 370/168 time (CPU) and almost a half megabyte (448K bytes with some paging under VS) of main memory. This is a task obviously beyond the reach of a minicomputer facility.

The second major part of CROMIS, XMAP, for generating ROM images from XMAS intermediate output, was also installed in a similar manner. The entire microcode for X77, written and debugged using A3076/S3076 package on the KAIS NOVA facility as described later, was processed with a minor modification using CROMIS on the SLAC triplex to obtain ROM programming files, for use with Intel MDS based hardware tools described subsequently.

3. A cross-assembler for PACE (in FORTRAN). During the initial stage of X77 only short programs in PACE language were needed for testing purposes. As the hardware realization of X77 system nears the need for PACE programs of substantial lengths will arise. Therefore a major effort will be directed toward expanding this cross-assembler by providing features suitable for developing large programs such as generation of modular relocatable object codes.

The software mentioned above, Items 1 through 3, were used in a combined manner illustrated in Fig. 1 The total system may run in a batch mode optionally generating a detailed printout of machine states including register contents, data, function, and control bus signals at each micro-instruction cycle. This system proved to be indispensible in debugging the hardware as well as the microcode.

4. The software tools for X77 included other miscellaneous programs such as that for preparing a wire-wrapping list. The task involves, given a list of independent connections pairs specified using logical names for pins of ICs and other components more convenient for circuit diagrams, translating to physical names related to their physical layout on a board, grouping into "chain" lists of pins connected together, and determining pins without connections. From a programming point of view such a task as described is relatively simple to implement. But the author has witnessed in an environment of a large engineering laboratory that several man-days of wire-wrapping had to be abandoned because such a preparatory task was by-passed.

3.2 Hardware Tools.

The hardware facility acquired for use in X77, which require mentioning because of their unique usefulness, include:

5. Intel MDS-ICE-30 3000 Series In-Circuit Emulator[7] for "in-circuit" emulation of the 3001 Microprogram Control Unit[2], and

6. Intel SIM-104 ROM Simulators[8], which using high speed RAM simulates 3604 and 3624 electrically programmable read-only memory in a user specifiable configuration.

These devices are supplied by Intel as modules to be resident in the Intellec MDS Microcomputer Development System, a complete configuration of which has been acquired and installed at KAIS Project Micro Laboratory. The availability of such a development system and particularly of items 5 and 6 mentioned above was a major factor in deciding on the 3000 Series as opposed to others[9].

4. Input/Output.

The X77 CPU module is only a subsystem of a functioning computer system. Approaches taken concerning the other subsystems required, their stage of development ranging from a mere background research to actual implementation, are briefly described below.

The X77 16-bit CPU module is coupled through

a shared memory (for message buffers) and interrupts with another CPU module based on the 8-bit microprocessor 8080, whose purpose is to serve as an autonomous input/output processor. The ensuing advantages are manifold:

a. Another part of Project Micro has been engaged for several years in experiments related to a "personal" microcomputer system centered around the 8080 processor including a variety of pheripheral devices. In addition, an extensive software support related to 8080 processor is available in Project Micro, such as A8076/S8076 cross-assembler/simulator package for 8080 running on the KAIS NOVA facility and the resident PL/M compiler running on the Micro Laboratory MDS system All of these facilities will be immediately available to X77. The idea for such solution is of course not new; For example, in the BRUSH project[10] at Max-Planck Institute, Munich, which the author participated several years ago, involving the design and construction of a fast digital computing system (using conventional TTL circuits) the input/output problem was solved by coupling the system to a PDP-8 (Digital Equipment Corp).

b. The organization mentioned for X77 allows a concurrent processing of internal and external processes corresponding roughly to program execution in the X77 CPU and input/output in the 8080 processor respectively.

c. Design of monitors supervising inter-process communications and coordinating such concurrent processing in the scale of X77 provides opportunities for challenging yet manageable experiments.

5. Systems Software.

The development of systems software including compilers for high level languages traditionally lagged that of hardware. Thus, it is not surprising that the current state of systems software for microprocessors is yet dismal. With the accelerating pace in power and variety of new microprocessors introduced it is inevitable that the problem of developing and maintaining software, systems — as well as application-type, is becoming ever more acute and new approaches in software design and implementation have to be sought In the recent past significant progress has been achieved in software methods, particularly in the area of programming languages and their compilers. Project Micro is devoting more than half of its manpower and other resource to obtaining practical results in the scale of X77 pertaining to systems software based on these knowledge. This aspect of Project Micro will be described in subsequent reports.

6. Results.

As of this writing X77 CPU design and the first version of microcode has been completed and debugged to a substantial extent using the P8076 simulation package. A preliminary result thus obtained indicates that compared to PACE (running at the maximum clock frequency of 2 MHz) X77 CPU (with the micro-instruction cycle time of 200 nsec) achieves about 5 times the speed enhancement; macro-instruction execution time ranging from 1.4 μsec (for RAND) to 2.0+0.4n μsec (for SHR with shift count of n) not including main memory access time. The comparable times for PACE are 8 and 16+6n μsec respectively.

The CPU prototype has been wire-wrapped and is in the process of being debugged using the MDS facilities mentioned earlier. The design and prototyping of the input/output subsystem is in progress.

Details concerning various phases of X77 as described above together with results being obtained will be presented subsequently.

In summary Project X77 is essentially experimental in character with a principal emphasis placed on the actual construction of a working prototype. And as with any experimental project in engineering it has requires — and continues to do so — a collaboration of many individuals — graduate students or otherwise — associated with Project Micro Laboratory at KAIS. Two of those who had past association having made major contributions to X77 as part of their M.S. thesis work at KAIS are Il Soo Ahn[11] with the task of CPU design and microcoding and Chang Hoon Lee[12] with that of implementing A3076 micro-assembler.

Finally even though there is an abundance of literature dealing with various conventional aspects of microprogramming[13] few of them appear immediately relevant to practical applications of LSI bit-slice processors, and there does not appear to be much need for an apology on the part

of the author for the singular lack of a long list of references.

References and Footnotes.

1. J. C. H. Park, Microprocessors, Journal of Korean Institute of Electrical Engineers, 25, 535 (1976).
2. Intel Series 3000 Reference Manual, Intel Corp. (1976).
3. PACE Technical Description, National Semiconductor Corp. (1975).
4. Currently most of these in wide use are 8-bit microprocessors so that in terms of throughput PACE with its 16-bit wide data path and richer instruction set is competitive.
5. Subsequently it came to our attention that National Semiconductor Corp. is producing in 1977 a single-board implementation using Schottky TTL of PACE μP, called "Super-PACE". An interesting direct comparison is now possible.
6. Intel Series 3000 Microprogramming Manual, Intel Corp. (1976).
7. ICE-30 In-Circuit Emulator Reference Manual Intel Corp. (1975).
8. ROM-Simulator Reference Manual, Intel Corp. (1975).
9. Such as Advanced Micro Devices 2900 Bipolar Microprocessor Family.
10. A.J. Flavell, F. Gandini, J. Park, R. Ruediger, R. Schilling, L. Schnupp, BRUSH Status Report, Max-Planck-Institut fur Physik und Astrophysik, Abt. Numerische Rechenmaschinen, Munich, Germany (1972).
11. Il-Soo Ahn, Emulation with the Microprogrammable Microprocessor, a thesis submitted to KAIS for M.S. in Electrical Engineering (1976).
12. Chang-Hoon Lee, Design and Implementation of Micro-Assembler and General Purpose Macro-generator, a thesis submitted to KAIS for M.S. in Basic Science (1976)
13. See for instance L.H. Jones, An Annotated Bibliography of Microprogramming, SIG MICRO Newsletter, 7, 95 (1976).

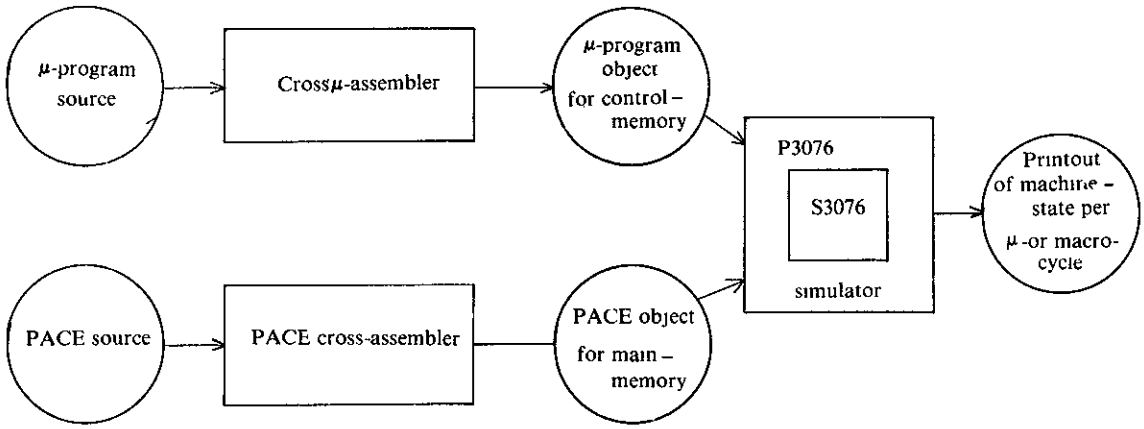

Fig. 1. Cross-assemblers and Simulator for X77